Non-US GR 6

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-144608
(43)Date of publication of application : 25.05.2001

(51)Int.CI. H03L 7/093
H03L 7/099

(21)Application number : 11-323291
(22)Date of filing : 12.11.1999

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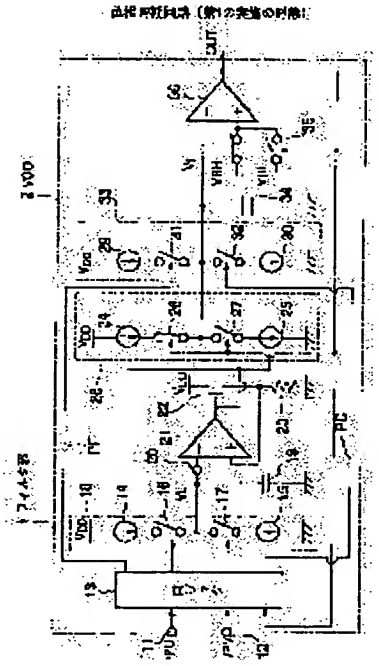
(54) PHASE SYNCHRONIZATION CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a phase synchronization circuit complying with a low power supply voltage and a high-speed processing that surely conducts phase locking when being employed for a PLL circuit.
SOLUTION: A logic circuit 13 of a filter section 1 generates a phase forward signal PF and a phase delay signal PD from a lead signal/FU, a lag signal/PV and an output signal OUT of a VCO 2. A charge pump 28 of the VCO 2 supplies/extracts a current in response to an output voltage VL of the filter section 1 to/from a capacitor 34. Furthermore, the charge pump 33 supplies/extracts a current in response to the phase forward signal PF and the phase delay signal PD to/from the capacitor 34. The capacitor 34 is connected to a comparator 36, which is oscillated at a frequency correspondent to a voltage Vf across the capacitor 34.



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[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]